REMARKS

Claims 1-33 are pending in the present application and stand rejected. The Examiner's reconsideration is respectfully requested in view of the above amendment and the following remarks.

Claims 15 and 22 have been amended, as required by the Examiner, to correct minor informalities. Withdrawal of the objection to claims 15 and 32 is respectfully requested.

Claims 1-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Torii (U.S. Patent No. 6,122,712) in view of Steckermeier et al ("Using Locality Information in Userlevel Scheduling) (hereinafter "Steckermeier"). The rejection is respectfully traversed.

The Examiner's arguments are legally deficient for at least the following reasons.

The Office Action cites col.3, lines 47-56 of Torii as teaching or suggesting "storing in a first data structure thread ids for at least some of the threads associated with a context switch performed by the operating system, each of the thread ids uniquely identifying one of the threads." Applicants disagree.

The recited portion of Torii teaches a thread management unit that "manages the *generation and the eliminating of threads*." The thread management unit simply allocates IDs in order of *generation* of the threads. The recited portion of Torii does not teach of suggest that the IDs refer to "threads associated with a context switch performed by the operating system." Thus, the recited portion of Torii does not teach or suggest "storing in a first data structure thread ids for at least some of the *threads associated with a context*

switch performed by the operating system, each of the thread ids uniquely identifying one of the threads," as claimed in claim 1.

For future reference in other arguments below, it is established that the Office Action argues that the "thread identifier register 5," as disclosed in Torii, teaches or suggests the "first data structure," as claimed in claim 1. Solely for the sake of argument, this will be assumed to be true below.

The Office Action cites col. 8, line 36-col. 9, line 32 of Torii as disclosing "storing in a second data structure a plurality of entries for a plurality of groups of contiguous cache lines, each of the plurality of entries arranged such that a thread id in the first data structure is capable of being associated with at least one of the contiguous cache lines in at least one of the plurality of groups of contiguous cache lines, the thread identified by the thread id having accessed the at least one of the contiguous cache lines in the at least one of the plurality of groups of contiguous cache lines."

The Examiner has cited a long passage to disclose a large portion of claim 1 in lieu of addressing each and every limitation of the claim. Thus, Applicants are left to *guess* as to which portions of the recited portion of Torii teach or suggest the various limitations in claim 1. It is respectfully reminded that the Examiner must address each and every limitation claim.

The recited portion Torii does not teach or suggest "storing in a second data structure a plurality of entries for a plurality of groups of contiguous cache lines," as claimed in claim 1. It is unclear to Applicants which part of the recited portion of Torii teaches or suggests the "second data structure." In any case, the recited portion of Torii does not teach or suggest "each of the plurality of entries arranged such that a *thread id in*

the first data structure is capable of being associated with at least one of the contiguous cache lines in at least one of the plurality of groups of contiguous cache lines," as claimed in claim 1. The recited portion of Torii does not make reference to the "thread identifier register 5," which, as noted above, is what the Examiner argues teaches or suggest the "first data structure."

It is also submitted that the recited portion of Torii does not teach or suggest "the thread identified by the thread id having accessed the at least one of the contiguous cache lines in the at least one of the plurality of groups of contiguous cache lines," as claimed in claim 1.

The Office Action cites §3.2 and §3.2.2 of Steckermeier as teaching or suggesting "mining for patterns in the plurality of entries in the second data structure to locate multiples of a same thread id that repeat with respect to at least two of the plurality of groups of contiguous cache lines." Neither § 3.2 nor § 3.2.2 teach or suggest "mining for patterns." Steckermeier is concerned with distributing threads on available processors based on hints by a programmer or compiler. It is respectfully asserted that Steckermeier is entirely unrelated to "*mining* for patterns...to locate multiples of a same thread id that repeat with respect to at least two of the plurality of groups of contiguous cache lines," as claimed in claim 1.

Even assuming, *arguendo*, that the Torii and Steckermeier disclose the limitations of claim 1 as argued by the Examiner, it is respectfully submitted that Torii and Steckermeier cannot be properly combined without improper hindsight knowledge. For a motivation to combine, the Examiner states "[t]he combination of Torii and Steckermeier provide a complete model of how to represent data patterns and utilize them to reduce

cache misses and increase the performance of a system." The mere fact that the prior art could be modified as proposed by the Examiner is not sufficient to establish a *prima facie* case of obviousness. *See In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). The Examiner must explain why the prior art would have suggested to one of ordinary skill in the art the desirability of the modification. *See Fritch*, 972 F.2d at 1266, 23 USPQ2d at 1783-84. By simply stating a generic benefit, the Examiner has failed to cite evidence *in the prior art* that the suggestion to modify the cited references as proposed by the Examiner exists. It can only be assumed that the motivation to combine is derived from the instant application.

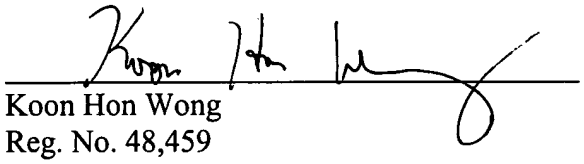
With regard to claim 16, § 3.2 of Steckermeier does not teach or suggest "*mapping* the threads identified by the located multiples of the same thread id to at least one native thread."

With regard to claim 33, § 3.2.2 of Steckermeier does not each or suggest "*identifying pools of threads* in the plurality of entries in the second data structure such that each of the pools of threads comprises the threads identified by a same thread id that forms a multiple with respect to one of the plurality of groups of contiguous cache lines, the multiple repeating with respect to at least two of the plurality of groups of contiguous cache lines."

Accordingly, independent claims 1, 16 and 33 are believed to be patentably distinguishable over the combination of Torii and Steckermeier. Dependent claims 2-15 and 17-32 are believed to be allowable for at least the reasons given for claims 1 and 16. Withdrawal of the rejection of claims 1-33 is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

By: 

Koon Hon Wong
Reg. No. 48,459
Attorney for Applicants

F. CHAU & ASSOCIATES, LLC
130 Woodbury Road
Woodbury, NY 11797
Telephone: (516) 692-8888
Facsimile: (516) 692-8889